17. (Amended) The method of claim 14, wherein implanting dopant atoms into said gate electrode layer to define a layer of dopant material in said gate electrode layer comprises implanting dopant atoms into said gate electrode layer to define a layer of dopant material in said gate electrode layer, said layer of dopant material defining a region of said gate electrode layer that is positioned between said layer of dopant material and said gate dielectric layer.

REMARKS

As an initial matter, Applicants reaffirm election to prosecute claims 1-20. Claims 7, 8, 16, and 17 have been amended. No new matter has been added. Thus, claims 1-20 remain pending in the present application.

In the Office Action, the drawings were objected to as not showing every feature specified in the claims. In particular, the Examiner alleges that the drawings do not show the claimed feature of "at least a portion of said layer of dopant material being in contact with said gate dielectric layer." Applicants submit herein a proposed Figure 6 that shows the claimed feature of "at least a portion of said layer of dopant material being in contact with said gate dielectric layer." Applicants respectfully submit that the proposed drawing does not contain new matter. For example, in Figures 3 and 4, a region 47 is shown interposed between the gate dielectric layer 40 and the layer of dopant material 48. However, it is stated that "the region 47, if it exists at all, may become vanishingly thin." See Patent Application, pg. 9, ll. 23-24 and Figures 3 and 4. In that case, at least a portion of said layer of dopant material 48 would be in contact with said gate dielectric layer 40, as claimed in claim 9. Applicants will submit a formal drawing and appropriate amendments to the specification upon receiving the Examiner's

approval of the proposed Figure 6 and an indication of allowable subject matter. Applicants respectfully request that the Examiner's objection be withdrawn.

In the Office Action, claims 7 and 16 were objected to because of informalities. Claims 7 and 16 have been amended solely to correct the informalities cited by the Examiner and, accordingly, the scope of claims 7 and 16 has not been narrowed by the aforementioned amendments. Applicants respectfully request that the Examiner's objections be withdrawn.

In the Office Action, claims 8 and 17 were rejected under 35 U.S.C. § 112, second paragraph, as allegedly being indefinite for failing to point out and distinctly claim the subject matter which Applicants regard as the invention. The Examiner's rejections are respectfully traversed. Claims 8 and 17 have been amended solely to clarify the claimed invention as suggested by the Examiner and, accordingly, the scope of claims 8 and 17 have not been narrowed by the aforementioned amendments. Applicants respectfully request that the Examiner's rejections of claims 8 and 17 be withdrawn.

In the Office Action, claims 1-8, 11-17, and 20 were rejected under 35 U.S.C. § 102(b) as allegedly being anticipated by Raicu (U.S. Patent No. 4,561,907). The Examiner's rejections are respectfully traversed.

With regard to independent claims 1 and 14, Applicants describe and claim forming a gate dielectric layer above a semiconductor substrate, forming a gate electrode layer above said gate dielectric layer, and implanting dopant atoms into said gate electrode layer to define a layer of dopant material in said gate electrode layer. Applicants further describe and claim patterning at least said gate electrode layer to define a gate electrode comprised of a plurality of sidewalls, said sidewalls having a recess formed therein.

Raicu is understood to be directed to forming vertical sidewall profiles using a process that includes rapid thermal annealing, Raicu, however, does not describe or suggest Applicants' claimed process. For example, Raicu describes a lightly doped polysilicon layer 62 formed above a substrate 43, a highly-doped polysilicon layer 61 formed above the lightly doped polysilicon layer 62, and an etch mask 42. The highly doped polysilicon layer 61 may be undercut during an etch process. See Raicu, col. 9, ll. 20-32 and Figure 7. However, in this example, Raicu does not disclose forming a gate dielectric layer above the semiconductor substrate or forming a gate electrode layer above the gate dielectric layer. For another example, Raicu describes etching a polysilicon layer (not shown) to form a gate 111 having a desired vertical sidewall. See Raicu, col. 11, ll. 9-12 and Figure 14. However, in this example, Raicu does not describe patterning at least a gate electrode layer to define a gate electrode comprised of a plurality of sidewalls, said sidewalls having a recess formed therein. Thus, Applicants respectfully submit that the present invention is not anticipated by Raicu and request that the Examiner's rejection of claims 1-8, 11-17, and 20 under 35 U.S.C. § 102(b) be withdrawn.

Moreover, it is respectfully submitted that the present invention is not obvious in view of Raicu. To establish a *prima facie* case of obviousness, three basic criteria must be met. First, the prior art reference (or references when combined) must teach or suggest all the claim limitations. *In re Royka*, 490 F.2d 981, 180 U.S.P.Q. 580 (CCPA 1974). Second, there must be some suggestion or motivation, either in the references themselves or in the knowledge generally available to one of ordinary skill in the art, to modify the reference or to combine reference teachings. That is, there must be something in the prior art as a whole to suggest the desirability, and thus the obviousness, of making the combination. *Panduit Corp. v. Dennison Mfg. Co.*, 810 F.2d 1561 (Fed. Cir. 1986). In fact, the absence of a suggestion to combine is dispositive in an

obviousness determination. *Gambro Lundia AB v. Baxter Healthcare Corp.*, 110 F.3d 1573 (Fed. Cir. 1997). The mere fact that the prior art can be combined or modified does not make the resultant combination obvious unless the prior art also suggests the desirability of the combination. *In re Mills*, 916 F.2d 680, 16 U.S.P.Q.2d 1430 (Fed. Cir. 1990); M.P.E.P. § 2143.01. Third, there must be a reasonable expectation of success. The teaching or suggestion to make the claimed combination and the reasonable expectation of success must both be found in the prior art, and not based on applicant's disclosure. *In re Vaeck*, 947 F.2d 488, 20 U.S.P.Q.2d 1438 (Fed. Cir. 1991); M.P.E.P. § 2142. A recent Federal Circuit case emphasizes that, in an obviousness situation, the prior art must disclose each and every element of the claimed invention, and that any motivation to combine or modify the prior art must be based upon a suggestion in the prior art. *In re Lee*, 61 U.S.P.Q.2d 143 (Fed. Cir. 2002) (copy attached). Conclusory statements regarding common knowledge and common sense are insufficient to support a finding of obviousness. *Id.* at 1434-35.

With regard to independent claims 1 and 14, the cited prior art contains no suggestion or motivation to modify Raicu to arrive at the claimed invention. In fact, Raicu teaches directly away from Applicants' invention, *i.e.* patterning at least a gate electrode layer to define a gate electrode comprised of a plurality of sidewalls, said sidewalls having a recess formed therein. For example, Raicu teaches that undercutting is an inherent problem that is highly undesirable. Raicu further teaches that undercutting is a consequence of the undesirable isotropic etch characteristics of highly doped silicon. See Raicu, col. 3, ll. 26-46. To remedy the inherent problem of undercutting, Raicu teaches heat pulse annealing silicon, such as the gate 111, and then etching the silicon in the presence of an etching mask (not shown) to provide the desired vertical sidewall profile to the gate 111. See Raicu, col. 11, ll. 1-12 and Figures 13 and 14.

In the Office Action, claims 9 and 18 were rejected under 35 U.S.C. § 103(a) as allegedly being unpatentable over Raicu in view of Han (U.S. Patent No. 6,103,603). Claims 9 and 18 recite a layer of dopant material in contact with the gate dielectric layer. The Examiner relies on Han for a teaching to form a layer of dopant material that is in contact with a dielectric layer. However, Han does not remedy the aforementioned deficiencies in the primary reference with regard to independent claims 1 and 14. Since claims 9 and 18 depend from claims 1 and 14, respectively, Applicants respectfully submit that the claims 9 and 18 are not obvious over Raicu in view of Han. Withdrawal of the Examiner's rejections of 9 and 18 under 35 U.S.C. § 103(a) is respectfully requested.

Claims 10 and 19 were rejected under 35 U.S.C. § 103(a) as allegedly being unpatentable over Raicu. The Examiner's rejections are respectfully traversed. Claims 10 and 19 set forth specific dopant concentrations. The Examiner alleges that the recited dopant concentrations would have been obvious to one of ordinary skill in the art. However, claims 10 and 19 depend from claims 1 and 14, respectively. Thus, for at least the aforementioned reasons, Applicants respectfully submit that the present invention is not obvious over Raicu. Withdrawal of the Examiner's rejections of 10 and 19 under 35 U.S.C. § 103(a) is respectfully requested.

For the aforementioned reasons, it is respectfully submitted that all claims pending in the present application are in condition for allowance. The Examiner is invited to contact the undersigned at (713) 934-4052 with any questions, comments or suggestions relating to the referenced patent application.

Respectfully submitted,

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AGENT FOR APPLICANTS

AMENDED CLAIMS FOR SERIAL NO. 09/676,197

7. (Amended) The method of claim 1, wherein implanting dopant atoms into said gate electrode layer to define a layer of dopant material in said gate electrode layer comprises implanting dopant atoms into said gate electrode layer to define a layer of dopant material in said gate electrode layer, said layer of dopant material being completely separate from said gate dielectric layer [of dielectric material].

8. (Amended) The method of claim 1, wherein implanting dopant atoms into said gate electrode layer to define a layer of dopant material in said gate electrode layer comprises implanting dopant atoms into said gate electrode layer to define a layer of dopant material in said gate electrode layer, said layer of dopant material defining a region of said gate electrode layer that is positioned between said layer of dopant material and said gate dielectric layer [electrode].

16. (Amended) The method of claim 14, wherein implanting dopant atoms into said gate electrode layer to define a layer of dopant material in said gate electrode layer comprises implanting dopant atoms into said gate electrode layer to define a layer of dopant material in said gate electrode layer, said layer of dopant material being completely separate from said gate dielectric layer [of dielectric material].

17. (Amended) The method of claim 14, wherein implanting dopant atoms into said gate electrode layer to define a layer of dopant material in said gate electrode layer comprises implanting dopant atoms into said gate electrode layer to define a layer of dopant material in said

gate electrode layer, said layer of dopant material defining a region of said gate electrode layer that is positioned between said layer of dopant material and said gate dielectric layer [electrode].